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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/436,882	11/09/1999	DON A. VAN DYKE	0100.9900960	7260

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/436,882	VAN DYKE, DON A.	
	Examiner	Art Unit	
	William M. Treat	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13,15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-13, 15, and 17-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-6, 8-13, 15, and 17-18 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-13, 15, and 17-18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Favor (WO 97/13194).

4. The rejection and arguments presented in the examiner's previous actions (Paper No. 5, mailed 12/16/02 and paper no. 8, mailed 11/5/03) continue and are hereby incorporated by reference. Applicant's arguments filed 2/5/04 have been fully considered but they are not persuasive.

5. Applicants have repeated their argument in relation to Favor that (a) Favor fails to teach "determining whether the at least one flag modification enable bit allows updating of at one least flag in response to executing the operational code" as found in independent claims 1 and 10. They have further argued in support of their oft-repeated argument (b) because Favor is directed to an entirely different problem, he has no need to make the determination; (c) because Favor teaches x86 instructions are converted by decode hardware to RISC instructions, he teaches away from the determination being made at execution time; and, (d) because Favor includes his flag modification enable bit in the field he terms the RegOp/opcode field, he does not teach an instruction containing data representing operational code and data representing at least one flag modification enable bit as is also found in claims 1 and 10. Applicants have also argued on behalf of claims 4 and 13 that (e) Favor does not teach "updating a flag register if the flag modification bit

is set to allow modification of a flag in the flag register," and on behalf of claim 5 that (f) Favor does not teach "evaluating the flag modification enable bit to preserve flag bit settings for variable length instructions that are emulated using the fixed native instructions," and on behalf of claims 9 and 18 that (g) Favor does not teach "emulating unconverted variable length x86 instructions."

6. As to 5(a), if applicant will reread the minimal material suggested by the examiner, he will see that Fig. 6A shows the RISC-type instruction format of Favor's invention for his instruction types listed from page 35, line 12 through page 36, line 16 and that each of these instructions contains "a single-bit set status field (SS) field 624 at bit location [9]" (page 35, lines 7-8). Also, on page 36 at lines 25-28, part of the suggested minimal reading, it states, "**For Ops in which the set status (SS) field 624 is set to 1, indicating that this op does modify flags**, the extension field (EXT) 614 specifies four status modification bits designating the groups of flags that are modified by the Op." Finally, on page 38 at lines 7-9, part of the suggested minimal reading, it states, "Decoupling of condition code handling from operation type, using the independent TYPE 612 and set status (SS) field 624, allows some operations to be defined which do not update the flags." Inherently, Favor's system must determine whether bit 624 is set when processing 612-type instructions and then will update at least one flag when the bit is set. Applicant seems to think because he has named his bit in his claims a "flag modification enabled bit" and not the set status (SS) field as Favor did that this somehow provides patentable distinction. It does not. A computer is a binary device. It does not care what applicant names his bit or what Favor names the bit. As with applicant's system, when the bit is set in Favor's system, the flag or flags will be updated, and when

the bit is not set, the flag or flags will not be updated. Also, the determination for the computer is whether the bit in the instruction, which permits modification of the flag or flag, is on or off. The same determination is being made in applicant's system as in Favor's no matter what words applicant chooses to describe it.

7. As to 5(b), Favor has instructions with a bit in them which determines whether a flag or flags will or will not be modified. Therefore, he makes the claimed determination whether or not his system solves other problems. (See paragraph 6, *supra*, for the details related to the determination.)

8. As to 5(c), the examiner made it clear in paragraph 6, *supra*, that Favor's flag modification bit (624) in his fixed length native instructions is evaluated to determine if flag bit settings will be preserved or modified. It is the native RISC-type instructions which are fed to the execution stage that are being evaluated. Applicant's argument related to decoding is specious and irrelevant.

9. As to 5(d), Favor's instruction does contain data representing operation code (Reg/OP) and data representing at least one flag modification enable bit (set status (SS) field 624). There is nothing in applicant's claim language which would require the fields to be entirely separate. Nor would such a claim be patentable. How one names fields and what one says one named field includes has nothing to do with how the computer's circuitry evaluates the bits of an instruction. Furthermore, were applicant to make such a claim modification and argue its uniqueness, there are many undergraduate textbooks on how one uses the bits of an instruction to signal the computer what is to be done. Such simple arrangements are merely design choices.

10. As to 5(e), see paragraph 6, *supra*.

11. As to 5(f), it is clear Favor is using his RISC-type instructions to emulate the behavior of the variable length x86 instructions (page 74, claim 1). Inherent in the proper emulation of the behavior of the x86 instructions is preservation of the proper status flag settings. Favor teaches a specific operation/instruction for modifying the status flags which provides for a bit to be used in determining whether or not to modify the status flag or flags (claim 3, page 74 which depends from claims 1 and 2 on page 74). Flavor is not flipping the set status bit-field of claim 3 on and off randomly. Inherently, it is being used to preserve the proper status flag values for the proper emulation of the x86 instructions as claimed by applicants.

12. As to 5(g), Favor does teach "emulating unconverted variable length x86 instructions" (page 8, lines 29-31).

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

14. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication should be directed to William M. Treat at telephone number 703 305 9699. The examiner works at home on Wednesdays

but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER